FIG. 1

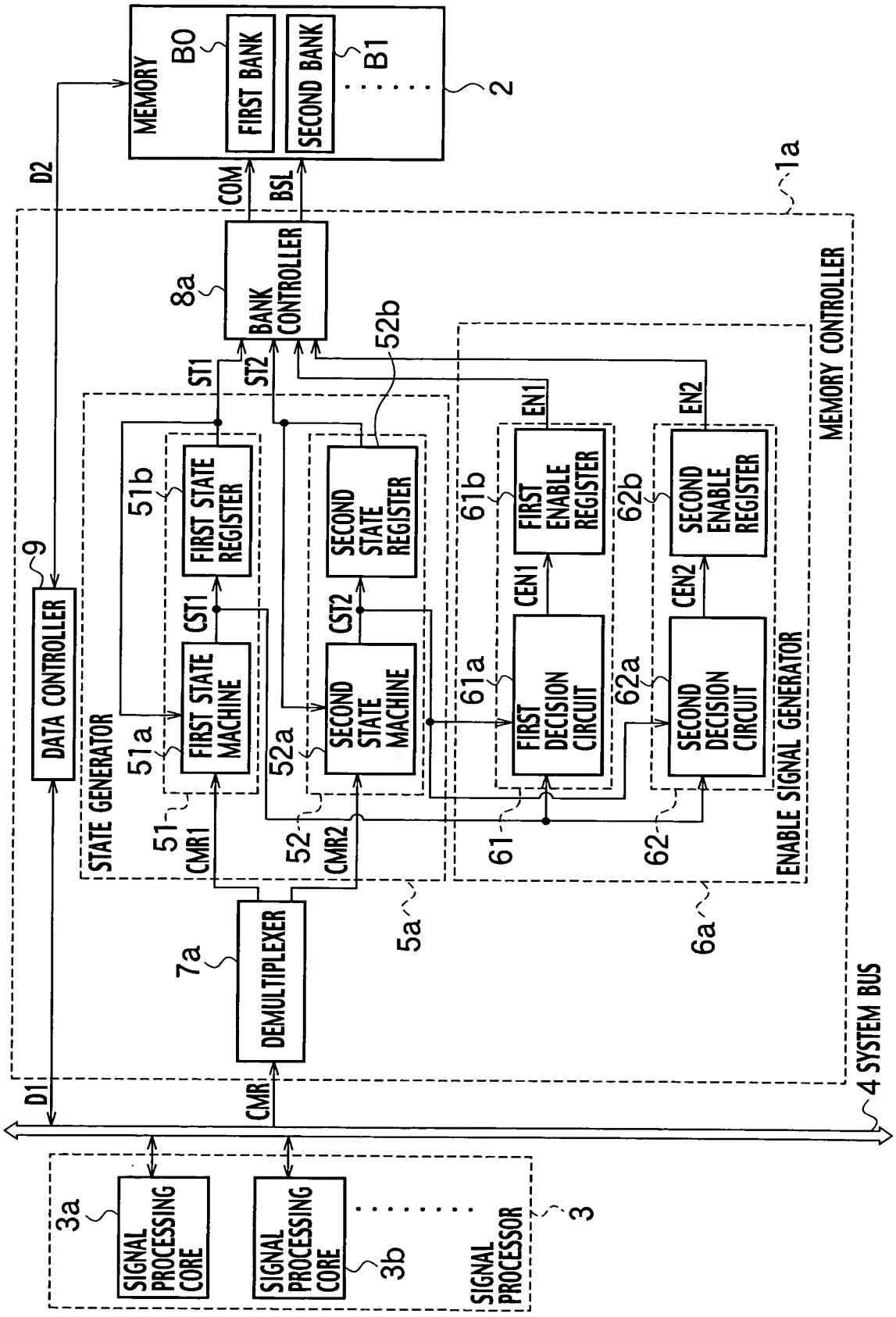

MEMORY
B0
FIRST BANK
SECOND BANK
B1
2
D2
COM
BSL
1a
8a
BANK CONTROLLER
ST1
ST2
52b
EN1
EN2
MEMORY CONTROLLER
9
DATA CONTROLLER
51b
FIRST STATE REGISTER
SECOND STATE REGISTER
61b
FIRST ENABLE REGISTER
62b
SECOND ENABLE REGISTER
CST1
CST2
CEN1
CEN2
STATE GENERATOR
51a
FIRST STATE MACHINE
52a
SECOND STATE MACHINE
61a
FIRST DECISION CIRCUIT
62a
SECOND DECISION CIRCUIT
ENABLE SIGNAL GENERATOR
51
CMR1
52
CMR2
61
62
5a
6a
7a
DEMULTIPLEXER
D1
CMR
4 SYSTEM BUS
3a
SIGNAL PROCESSING CORE
3b
SIGNAL PROCESSOR
3

FIG. 2

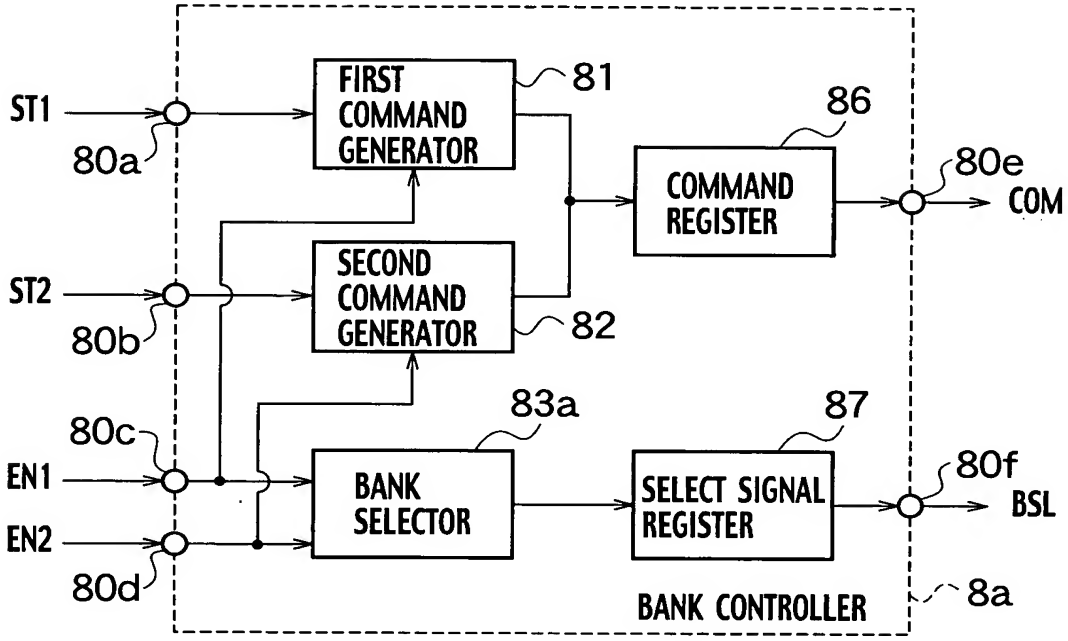


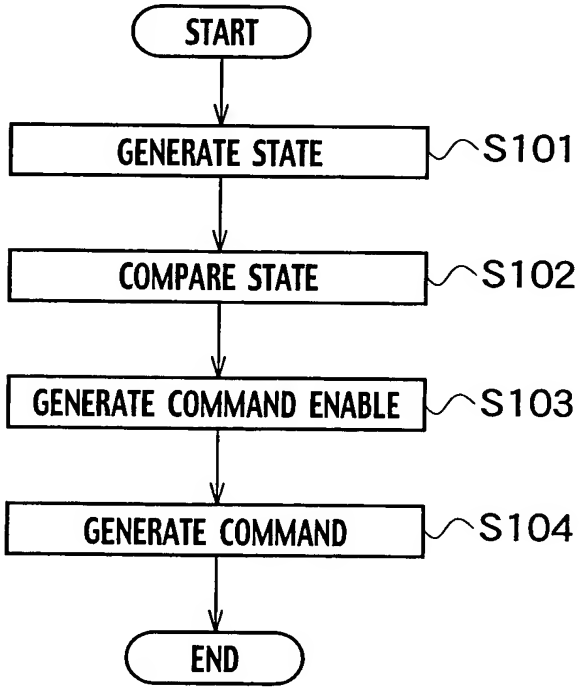
FIG. 3

CST1 / CST2	WAIT	ACTIVE	READ/WRITE	PRECHARGE
WAIT	0	1	1	1
ACTIVE	0	0	1	0
READ/WRITE	0	0	0	0
PRECHARGE	0	1	1	0

FIG. 4

CST1 / CST2	WAIT	ACTIVE	READ/WRITE	PRECHARGE
WAIT	0	0	0	0
ACTIVE	1	0	0	1
READ/WRITE	1	1	0	1
PRECHARGE	1	0	0	0

FIG. 5



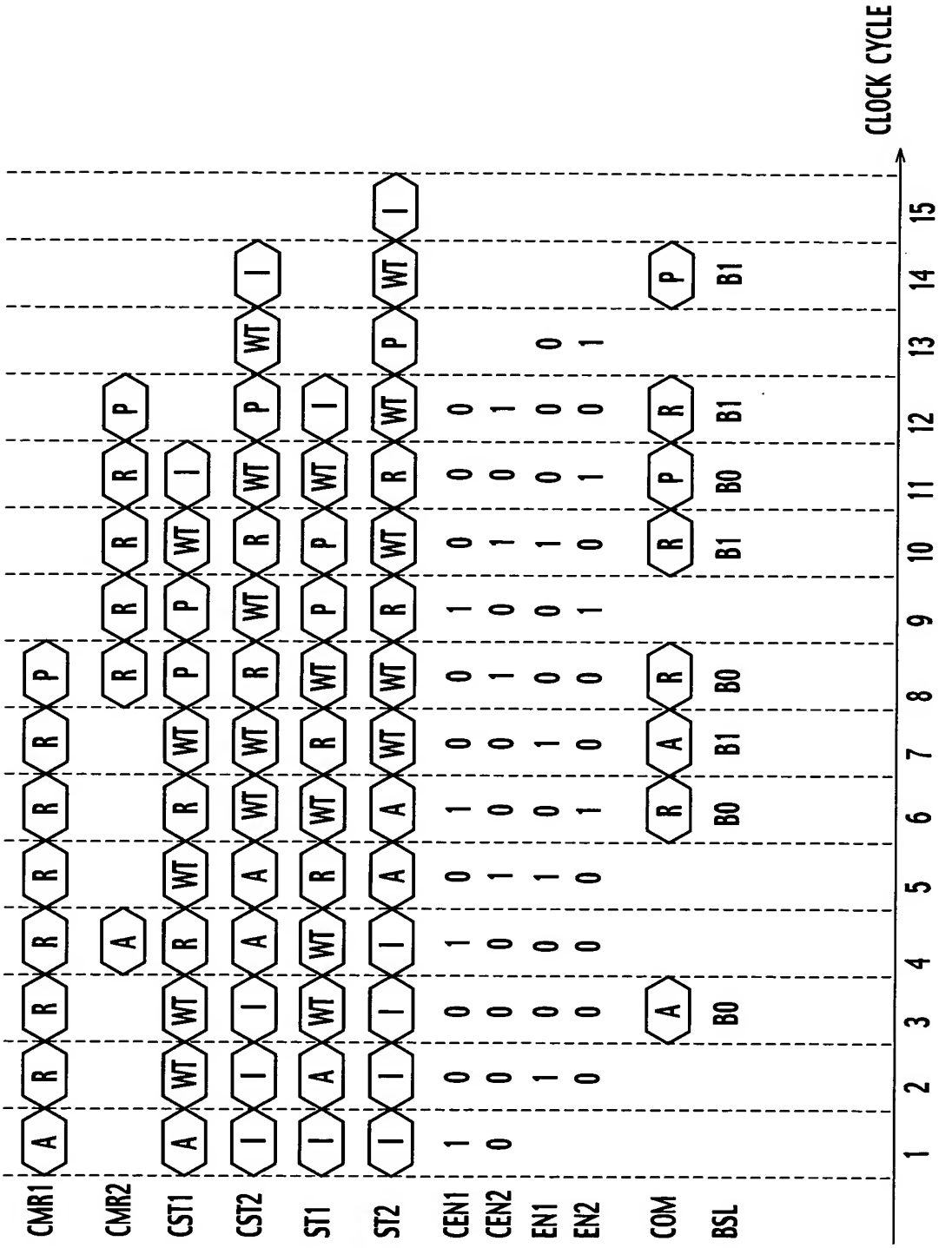


FIG. 6A
FIG. 6B
FIG. 6C
FIG. 6D
FIG. 6E
FIG. 6F
FIG. 6G
FIG. 6H
FIG. 6I
FIG. 6J
FIG. 6K
FIG. 6L

FIG. 7

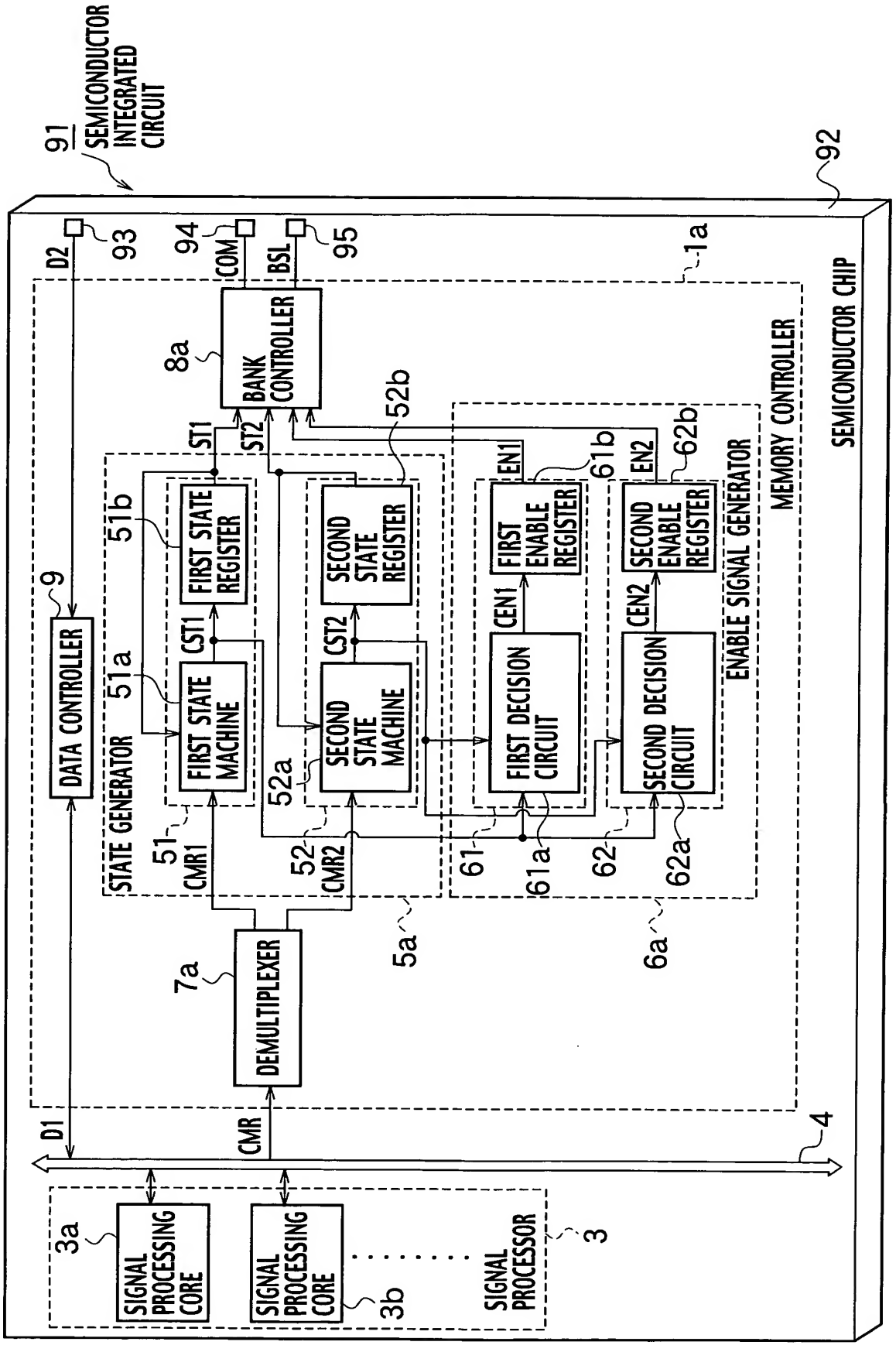

91
SEMICONDUCTOR INTEGRATED CIRCUIT
92
SEMICONDUCTOR CHIP
D2
93
94
COM
BSL
95
1a
MEMORY CONTROLLER
8a
BANK CONTROLLER
ST1
ST2
52b
EN1
61b
EN2
62b
9
DATA CONTROLLER
51b
FIRST STATE REGISTER
SECOND STATE REGISTER
FIRST ENABLE REGISTER
SECOND ENABLE REGISTER
51a
CST1
CST2
CEN1
CEN2
FIRST STATE MACHINE
SECOND STATE MACHINE
FIRST DECISION CIRCUIT
SECOND DECISION CIRCUIT
ENABLE SIGNAL GENERATOR
STATE GENERATOR
52a
51
CMR1
52
CMR2
61
61a
62
62a
5a
6a
7a
DEMULTIPLEXER
D1
CMR
4
3a
SIGNAL PROCESSING CORE
SIGNAL PROCESSING CORE
3b
SIGNAL PROCESSOR
3

FIG. 8

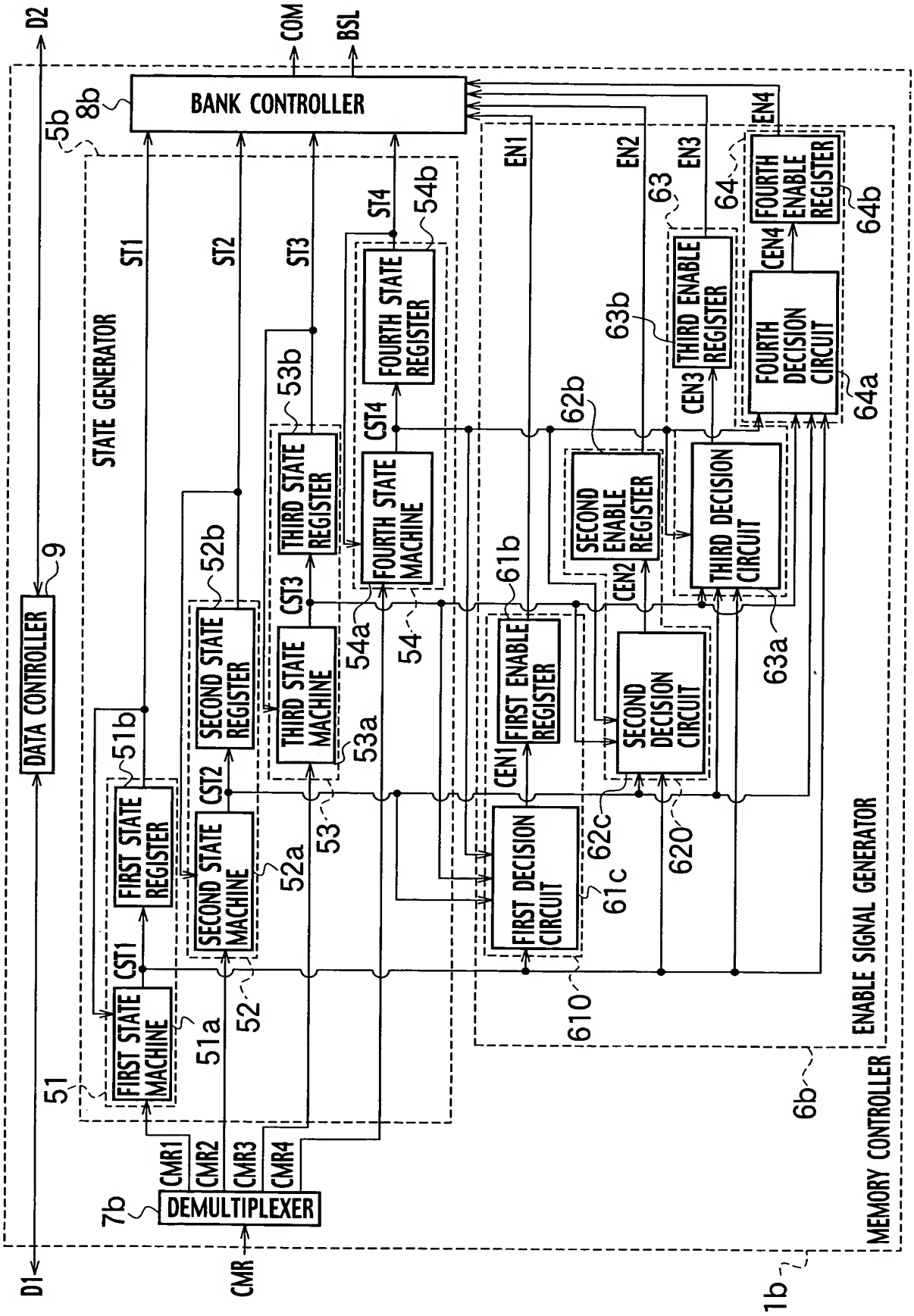
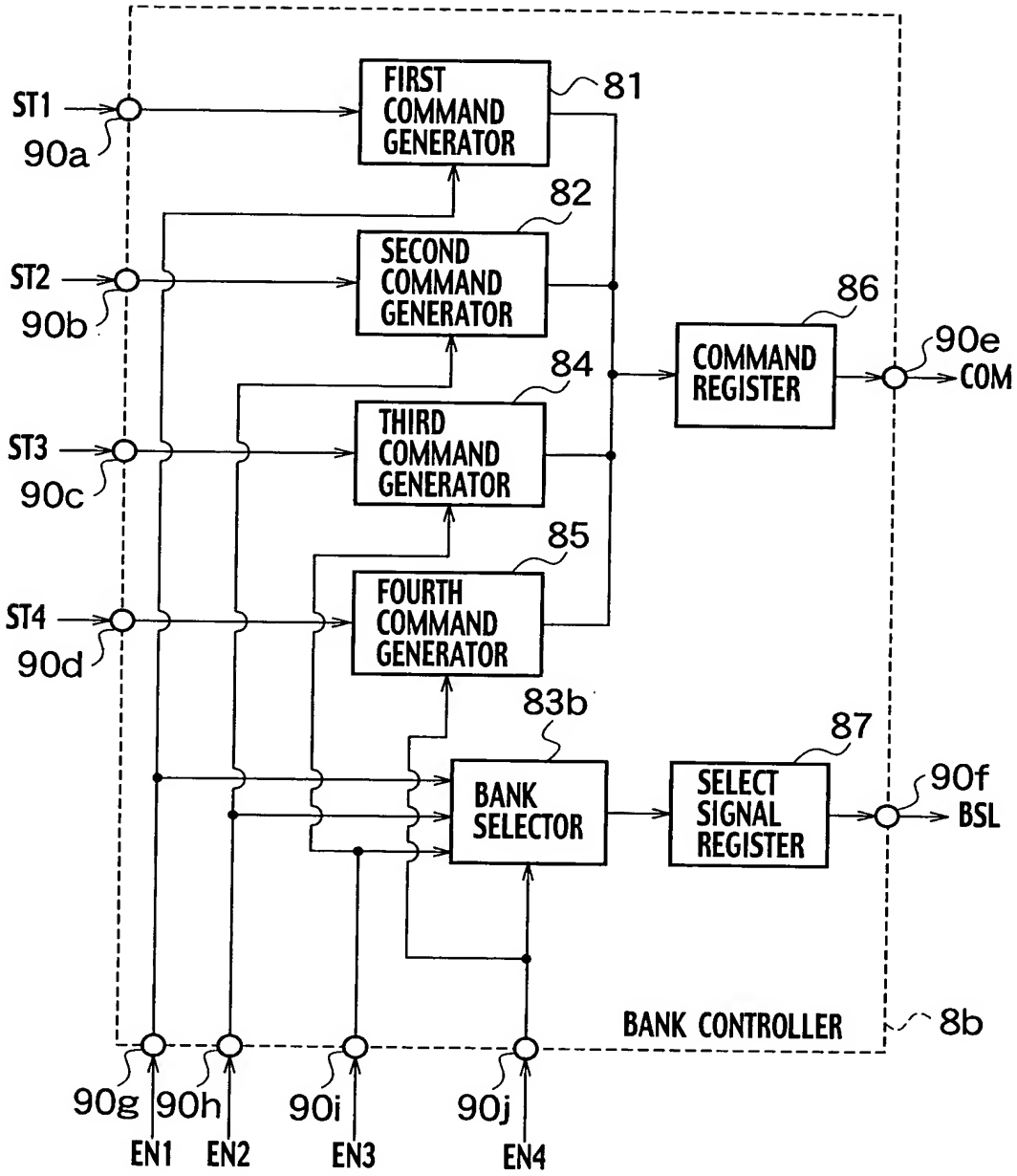

D2
COM
BSL
BANK CONTROLLER
8b
5b
STATE GENERATOR
ST1
ST2
ST3
ST4
54b
FOURTH STATE REGISTER
FOURTH STATE MACHINE
53b
THIRD STATE REGISTER
THIRD STATE MACHINE
52b
SECOND STATE REGISTER
SECOND STATE MACHINE
51b
FIRST STATE REGISTER
FIRST STATE MACHINE
DATA CONTROLLER
9
CST1
CST2
CST3
CST4
51a
52a
53a
54a
51
52
53
54
CMR1
CMR2
CMR3
CMR4
7b
DEMULTIPLEXER
D1
CMR
EN1
EN2
EN3
EN4
63
64
FOURTH ENABLE REGISTER
64b
CEN4
FOURTH DECISION CIRCUIT
64a
63b
THIRD ENABLE REGISTER
CEN3
62b
SECOND ENABLE REGISTER
CEN2
THIRD DECISION CIRCUIT
63a
61b
FIRST ENABLE REGISTER
CEN1
SECOND DECISION CIRCUIT
62c
620
FIRST DECISION CIRCUIT
61c
610
ENABLE SIGNAL GENERATOR
6b
MEMORY CONTROLLER
1b

FIG. 9


ST1
90a
FIRST COMMAND GENERATOR
81
ST2
90b
SECOND COMMAND GENERATOR
82
ST3
90c
THIRD COMMAND GENERATOR
84
ST4
90d
FOURTH COMMAND GENERATOR
85
COMMAND REGISTER
86
90e
COM
83b
BANK SELECTOR
87
SELECT SIGNAL REGISTER
90f
BSL
BANK CONTROLLER
8b
90g
90h
90i
90j
EN1
EN2
EN3
EN4